EE/CprE/SE 491 WEEKLY REPORT 03
Oct 7 - Oct 13

Group number: **22**

Project title: **ReRAM Compute Asic Fabrication**

Client &/Advisor: **Cheng Wang & Henry Duwe**

Team Members/Role:

Ali Mannan
Tyler Kloser
Austin Miller
Vinicius Malaman Soares

- **Weekly Summary**

  - Completed the first module through to pre-check. Obtained a design philosophy for the op-amp (2-stage with current MOSFET current mirror). Set up VM for all group members.

- **Past week accomplishments**

  - Vinicius Malaman Soares: Met with VLSI faculty on advice and guidance for the design of the opAMP. Started the design of the opAMP using the skywater PDK.
  - Tyler Kloser: Looked into different characteristics for the ADC design
  - Ali Mannan: Installed Docker and integrated design of 1-bit DAC with Harness Through Efabless. Parasitic extraction issues fixed. Helped Vinicius with schematic for creating a 2-stage op-amp. Provided testbenches for the op-amp that test the characteristics we need to look at (mainly input range, slew rate, etc.)
  - Austin Miller: VM Setup with all our netid's as sudo users. Created schematic of 1T1R cell. Began layout of it with magic

- **Pending issues**
  - Tyler Kloser: N/A
  - Ali Mannan: Parasitic extraction significantly affected characterization of 1-bit DAC, will be one of the first things to look at when a fully working 1-bit build is being optimized
  - Austin Miller: Magic can't find my reram cell to instantiate, will hopefully sort soon (probably just need to point out where it is for magic)

- Vinicius Malaman Soares: Finish the design for the current mirror, serving as a Iref.

Individual contributions

NAME	**Individual Contributions** *(Quick list of contributions. This should be short.)*	**Hours this week**	**HOURS cumulative**
Tyler Kloser	Characterize different ADC Designs	3	21
Ali Mannan	Passed pre-check (final stage before manufacturing) for the 1-bit DAC, and fully characterized it.	6	30
Austin Miller	1T1R Schem made, set and reset sim. Started layout	5	27
Vinicius Malaman Soares	Met with VLSI faculty. Started the design of OpAMP, Finished the difference stage.	9	26

- **Comments and extended discussion** *(Optional)*

- **Plans for the upcoming week**

  Unless the advisors suggest otherwise, we intend on continuing work on the TIA for the project and the 1T1R design of a reRAM module. ADC designs will be considered for our application.

  - Ali Mannan: When a schematic for a 2-stage op-amp is received, the work on layout will be done and taken through to pre-check. Plan on assisting with TIA schematic design (which is just choosing feedback resistor/capacitor values) for our needs.
  - Tyler Kloser: Choose which ADC design will work best with our design that will not interfere with ReRAM memresistors
  - Austin Miller: Get layout of 1T1R completed and through precheck, possibly chat with Ali if magic isn't working
  - Vinicius Malaman Soares: Finish OpAMP design, get started on ADC with team

- **Summary of weekly advisor meeting**
  - This week we discussed further design details, such as forming and reforming of ReRAM cells, 1T1R configuration, bit-line & word-line setup, as well as OpAMP design doubts.
  - Also discussed some design concepts for characterizing and creating test platforms for components